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APPLICATION NOTE 3541

Troubleshooting Guide for the DS31256 HDLC Controller

This troubleshooting guide details users' most common difficulties with hardware, software, and other topics when using the DS31256 HDLC controller. A troubleshooting checklist will help determine the reason for a problem. Possible solutions are recommended.

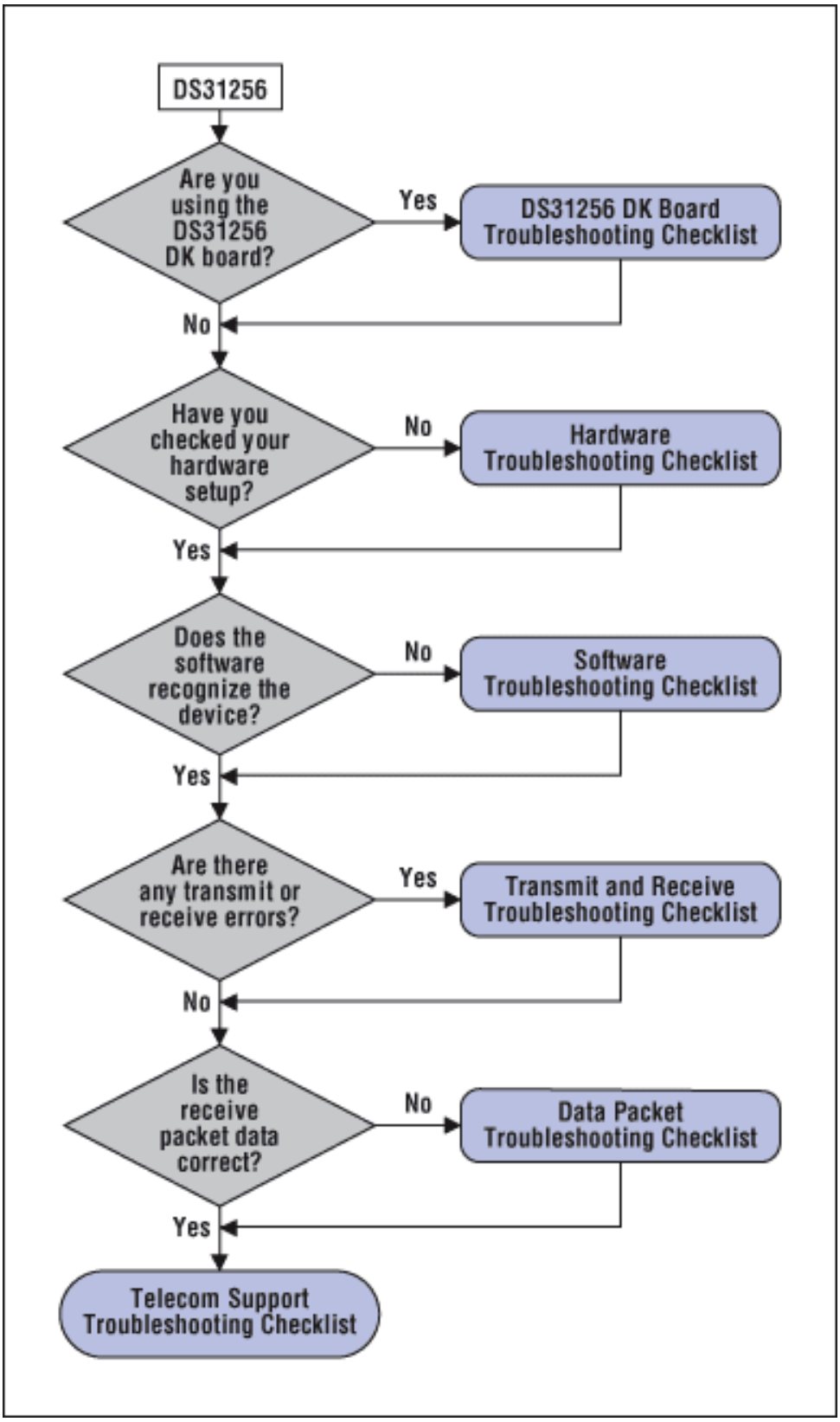
Overview

This application note describes several common difficulties that can occur when using the DS31256 HDLC controller. To assist in determining problem causes and reducing these difficulties, Dallas Semiconductor created this troubleshooting guide.

This troubleshooting guide helps verify the cause of a problem by narrowing down the debugging process. The guide suggests possible solutions and leads the user in the right direction to solving the problem. The most common difficulties in hardware, software, and other areas are listed; a helpful checklist and reminders for the user are included.

If this troubleshooting guide does not help resolve the problem, contact Dallas Semiconductor Telecom Support at telecomsupport@dalsemi.com.

Troubleshooting Flowchart. Please check the command boxes.



DS31256 DK Board Troubleshooting Checklist

- DIP switch settings—Verify that the board's DIP switch (see #1 in the picture below) settings are correct for the selected mode. Please refer to the DS31256 DK datasheet, Figure 1.2 for more details about the DIP switch settings.
- Oscillators—The two DK oscillators (see #2 in the picture below) provide timing to the HDLC ports. Remember to match the HDLC clock calculation with Figure 1B in the DS31256 DK datasheet.

- Device—Verify that the device is properly seated in the socket with the correct pin orientation (see #3 in the picture below).

Hardware Troubleshooting Checklist

- Verify hardware setup/connection—Check hardware such as the cable connection, or use the network loopback mode to test the device interconnections to ensure that all devices are setup correctly.
- Verify DS31256 part orientation on board.
- Verify that DS31256 is connected to a 3.3V supply.
- Verify that DS31256 is receiving PCI clock.
- Verify that DS31256 is receiving HDLC port clocks.
- Verify activity on PCI bus or local bus during register accesses.
- Verify DS31256 solder connections.
- Does replacing the DS31256 part fix the problem?

Software Troubleshooting Checklist

- Applications note checklist
  The configuration procedures will affect the performance of the DS31256. Dallas Semiconductor created the following application notes to explain how to initialize and configure the device. One application note presents the example code for implementing a register dump that will collect the configuration data for debugging purpose.
  - Application Note 2867: Initialization Steps for the DS31256 to configure the DS31256
  - Application Note 2872: Step-by-Step Configuration for Bridge Mode (DS31256)
  - Application Note 2871: Step-by-Step Configuration for Configuration Mode (DS31256)
  - Application Note 3295: DS31256 Envoy -- Example Code for Registers Dump
- Device limitations checklist
  - Did you try to use 64 E1 data streams? The DS31256 supports up to 60 T1 or 64 E1 data streams.
  - All receive buffers must start on a DWORD aligned address, and must have a byte size that is a multiple of four. The DS31256 has no restrictions on the transmit side buffers.
  - The minimum packet size is two data bytes (not including the CRC).
  - The minimum size of the FIFO-linked list block is four blocks (64 bytes).
- Software application checklist
  Because the DS31256 is a software configuration device, the software developer normally will use structures or pointers to access or store the data. Sometimes problems are caused by a software error, such as an incorrect address access or the way buffers or descriptors are recycled. We recommend that you check the following

areas of the software.
    - DS31256 DMA data structures and memory allocation—Make sure that all data structures and memory allocation are created and will be used correctly. The system may crash if any pointer tries to access an unavailable or inaccessible address.
    - Overlapping data structures—Check the start and end addresses of each data structure to ensure that each is correct. As an example, verify that the start address of the next queue does not overlap with the end address of the previous queue.
    - Read/write pointer wraparound and definition of the queue end address—Calculate the start and end addresses correctly. Remember that the number of entries a queue can hold is based on the start and end addresses.
    - Receive free-queue entry size is two dwords. All other queue entries are one dword.
    - All receive buffers must start on a dword aligned address and all receive buffers must have a byte size that is a multiple of four.
    - All descriptors must be dword aligned.
    - Buffer or descriptor recycling—Has the buffer or descriptor been recycled correctly?
- Driver—Did the driver code detect the DS31256 correctly?
- PCI
    - Check DS31256 PCI configuration register settings.
    - Check the PCI bridge chip configuration.
- High-speed mode
    - Receive FIFO can receive garbage during chip configuration, which results in extra packets received after device initialization.
    - Check HDLC port clock vs. port-data edge alignment.

Transmit and Receive Troubleshooting Checklist

Please see the detail in Application Note 399: DS31256 Envoy Loopback Modes , if the loopback mode is used.

Try to send one packet on one HDLC channel in loopback mode and go through the following checklist. Then, repeat the same procedures with the setting below to verify that the transmission is working correctly in different scenarios.

- Multiple packets on a single HDLC channel
- A single packet on multiple HDLC channels
- Multiple packets on multiple HDLC channels

Transmit-Side Checklist

- Did the software zero and reset all registers before configuration?
- Transmit path enabled—Check that all necessary and transmit-side registers in Table 1 have been reset (zero) and configured correctly.
- Transmit pending queue—Check the transmit pending-queue read and write pointer. The read and write pointers should be equal if the queue is empty. If not, the pointers should have advanced the correct amount.
- Transmit done queue—Check transmit done-queue read and write pointer. The read and write pointers should be equal if the queue is empty. If not, the pointers should have advanced the correct amount.
- Buffer and packet chaining—Check that the linked list has been set up correctly. Especially when multiple buffers are used, verify that the linked list has been constructed correctly.
- Transmit done-queue entry packet status and errors—Check transmit done-queue descriptor dword 0; bits 26 to 28 for packet status. These three bits report the final status of an outgoing packet, including the error states.
- Transmit packet descriptor PV bit—Check that transmit packet descriptor dword 3; bit 16/Pending Descriptor Valid (PV) is cleared by the host software when the descriptor is recycled.
- Buffer and descriptor recycling—Verify that the buffer and descriptor are recycled correctly.
- Transmit status report—Check SDMA register to see if any error has been reported.

Receive-Side Checklist

- Did the software zero or reset all registers before configuration?

- Receive path enabled—Check that all necessary and receive side registers in Table 1 have been reset (zero) and configured correctly.
- Receive queue—Check the receive free-queue read and write pointers. The read and write pointers should be equal if the queue is empty. If not, the pointers should have advanced the correct amount.
- Receive done queue—Check the receive done-queue read and write pointers. The read and write pointers should be equal if the queue is empty. If not, the pointers should have advanced the correct amount.
- Buffer chaining—Check that the buffer linked list in software has been recycled correctly.
- Receive done-queue entry status and errors—Check the receive done-queue descriptor dword 0; bits 27 to 29 for the final status (includes the errors) of an incoming packet.
- Buffer and descriptor recycling—Verify that the buffer and descriptor are recycled correctly.
- Receive status report—Check SDMA to see if any error has been reported.

Table 1. DS31256 Configuration Registers Checklist

Offset/Address	Name	Bits Number	Registers Description	Data Sheet Section
Master Configuration Register				
0000	MRID	15-0	Master Software Reset	5.1
Layer One Registers (n = port number)				
01xx	RP[n]CR	15-0	Receive Port n Control Register	6.2
02xx	TP[n]CR	15-0	Transmit Port n Control Register	6.2
03xx	CP[n]RD	15-0	Channelized Port n Register Data	6.3
03xx	CP[n]RDIS.CHID0-6	6-0	DS0 Channel ID	6.3
03xx	CP[n]RDIS.CPRS0 CP[n]RDIS.CPRS1	9-8	00 to select Channelized DS0 data	6.3
			01 to select Receive Configuration	
			10 to select Transmit Configuration	
HDLC Registers				
0404	RHCD	3-2	Receive HDLC Channel Definition	7.2
0400	RHCDIS	7-0	Receive HDLC Channel Definition Indirect Select	7.2
0484	THCD	3-2	Transmit HDLC Channel Definition	7.2
0480	THCDIS	7-0	Transmit HDLC Channel Definition Indirect Select	7.2
DMA Registers				
0700	RFQBA0	31-0	Receive Free-Queue Base Address 0 (lower word)	9.2.3
0704	RFQBA1	15-0	Receive Free-Queue Base Address 1 (upper word)	9.2.3
0708	RFQEA	15-0	Receive Free-Queue End Address	9.2.3
070C	RFQSBSA	15-0	Receive Free Small Buffer Start Address	9.2.3
0710	RFQLBWP	15-0	Receive Free-Queue Large Buffer Host Write Pointer	9.2.3
0714	RFQSBWP	15-0	Receive Free-Queue Small Buffer Host Write Pointer	9.2.3
0718	RFQLBRP	15-0	Receive Free-Queue Large Buffer DMA Read Pointer	9.2.3
071C	RFQSBRP	15-0	Receive Free-Queue Small Buffer DMA Read Pointer	9.2.3

0730	RDQBA0	15-0	Receive Done-Queue Base Address 0 (lower word)	9.2.4
0734	RDQBA1	31-16	Receive Done-Queue Base Address 1 (upper word)	9.2.4
0738	RDQEA	15-0	Receive Done-Queue end Address	9.2.4
073C	RDQRP	15-0	Receive Done-Queue Host Read Pointer	9.2.4
0740	RDQWP	15-0	Receive Done-Queue DMA Write Pointer	9.2.4
0750	RDBA0	15-0	Receive Descriptor Base Address 0 (lower word)	9.2.2
0754	RDBA1	31-16	Receive Descriptor Base Address 1 (upper word)	9.2.2
0770	RDMACIS	10-0	Receive DMA Channel Configuration Indirect Select	9.3.5
0774	RDMAC	15-0	Receive DMA Channel Configuration	9.3.5
0790	RLBS	12-0	Receive Large Buffer Size	9.2.1
0800	TPQBA0	15-0	Transmit Pending-Queue Base Address 0 (lower word)	9.3.3
0804	TPQBA1	31-16	Transmit Pending-Queue Base Address 1 (upper word)	9.3.3
0808	TPQEA	15-0	Transmit Pending-Queue End Address	9.3.3
080C	TPQWP	15-0	Transmit Pending-Queue Host Write Pointer	9.3.3
0810	TPQRP	15-0	Transmit Pending-Queue DMA Read Pointer	9.3.3
0830	TDQBA0	15-0	Transmit Done-Queue Base Address 0 (lower word)	9.3.4
0834	TDQBA1	31-16	Transmit Done-Queue Base Address 1 (upper word)	9.3.4
0838	TDQEA	15-0	Transmit Done-Queue End Address	9.3.4
083C	TDQRP	15-0	Transmit Done-Queue Host Read Pointer	9.3.4
0840	TDQWP	15-0	Transmit Done-Queue DMA Write Pointer	9.3.4
0850	TDBA0	15-0	Transmit Descriptor Base Address 0 (lower word)	9.3.2
0854	TDBA1	31-16	Transmit Descriptor Base Address 1 (upper word)	9.3.2
0870	TDMACIS	11-0	Transmit DMA Channel Configuration Indirect Select	9.3.5
0874	TDMAC	0-15	Transmit DMA Channel Configuration	9.3.5
FIFO Registers				
0900	RFSBPIS	0-7	Receive FIFO Starting Block Pointer Indirect Select	8.2
0904	RFSBP	0-9	Receive FIFO Starting Block Pointer	8.2

0910	RFBPIS	0-7	Receive FIFO Block Pointer Indirect Select	8.2
0914	RFBP	0-9	Receive FIFO Block Pointer	8.2
0920	RFHWMIS	0-7	Receive FIFO High Water Mark Indirect Select	8.2
0924	RFHWM	0-9	Receive FIFO High Water Mark	8.2
0980	TFSBPIS	0-7	Transmit FIFO Starting Block Pointer Indirect Select	8.2
0984	TFSBP	0-9	Transmit FIFO Starting Block Pointer	8.2
0990	TFBPIS	0-9	Transmit FIFO Block Pointer Indirect Select	8.2
0994	TFBP	0-9	Transmit FIFO Block Pointer	8.2
09A0	TFLWMIS	0-7	Transmit FIFO Low Water Mark Indirect Select	8.2
09A4	TFLWM	0-9	Transmit FIFO Low Water Mark	8.2
PCI Registers				
0x004/0A04	PCMD0	31-0	PCI Command Status 0	10.2

Data Packet Troubleshooting Checklist

- Is the receive packet size smaller or bigger than the size of sent data packet?
  - DWORD aligned—All receive buffers must start on a dword aligned address and must have a byte size that is a multiple of four.
  - Minus the 16-bit or 32-bit CRC at the end of the packet if the receive CRC selection bits (RCRC0/ RCRC1) in RHCD register are set.
  - Every DS0 channel should be zeroed when the DS31256 is reset (even unused DS0 channels). The data packet may be lost because the incorrect DS0 channel number was not reset or cleared correctly.
  - Actual buffer size must be greater than, or equal to the size specified in the receive large or small buffer size registers.
  - The descriptor value of transmit side must match the number in transmit packet descriptor dword 1; bits16 to 28 (byte count).
  - The buffer should be linked correctly if the multiple buffer is used.
- Does the receive number of packets match the number of packets sent?
  - Possible garbage data in FIFO and see the detail and troubleshooting guide in Application Note 399: DS31256 Envoy Loopback Modes.
- Does the receive packet data not match the data sent?
  - Non-DWORD aligned buffer—All receive buffers must start on a DWORD aligned address. All receive buffers must have a byte size that is a multiple of four.
  - CRC error—Are the CRC setting in both transmit and receive the same?
  - Extra packets—Possible garbage data in FIFO; see the detail and troubleshooting guide in Application Note 399: DS31256 Envoy Loopback Modes.
  - HDLC channel or port DS0 assignment—Check that all HDLC channels or DS0 channels have been configured with the correct channel or DS0 number. The HDLC channel number starts from 1 and DS0 starts from 0. The unused DS0 channels need to be zeroed during the reset process.
  - FIFO linked list—Check the FIFO linked list for each HDLC channel. Is the link list circular constructed correctly without overlap?
  - FIFO size—Check the setting of FIFO high and low water mark. The minimum size of the link list chain is four blocks (64 bytes).
  - Big or Little Endian format—Check the setting of Master Configuration (MC) register bit 6 PBO (PCI Bus Orientation).

Telecom Support Troubleshooting Checklist

- If a problem persists after following the checklist in this troubleshooting guide, you are encouraged to contact the Telecom Support group. The Telecom Support team will need registers dump for further investigation and debugging. To help users collect the required information, Dallas Semiconductor created Application Note 3295 DS31256 Envoy -- Example Code for Registers Dump to provide the necessary functionality.

Conclusion

This application note is a troubleshooting guide to help the user to resolve DS31256 problems. The troubleshooting checklist will help the user determine the reason for the problem, and possible solutions are recommended.

If you have further questions about our HDLC controller products, please contact the Telecommunication Applications support team by email at: telecom.support@dalsemi.com or call 01-972-371-6555.

More Information

DS31256: QuickView -- Full (PDF) Data Sheet